

design ideas

Edited by Bill Travis and Anne Watson Swager

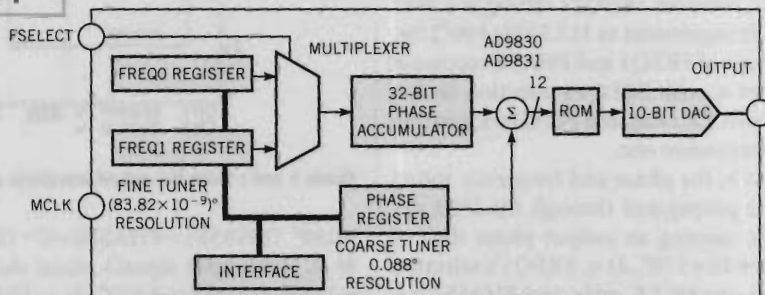
Scheme extends DDS phase-shift resolution

Mary McCarthy, Analog Devices Inc, Limerick, Ireland

DIRECT-DIGITAL-SYNTHESIS (DDS) devices find wide use in instrumentation and communications applications. Rather than using a baseband converter to modulate data in a communications system, you can use a DDS device. Such a device has onboard phase registers that accommodate phase-shift keying (PSK). In communications applications, the phase shifting is in steps of 45° ($\pi/4$ differential-quadrature PSK) or 90° (quadrature PSK). The device has enough resolution to generate these phase shifts. In instrumentation applications, the required phase shifts vary, depending on the system under development. Some applications require extremely accurate phase shifts. The phase registers in a DDS device are typically 12 bits wide, resulting in a phase resolution of $360^\circ/4096$, or 0.088° . However, by using the frequency register as in **Figure 1** to perform the phase-shifting, you can increase the phase-shifting resolution to 32 bits.

If the DDS device has two frequency registers, you can use one to generate the output signal and the other to generate the phase shifts. By using the frequency register to perform phase-shifting, the

Figure 1



By using both the phase and frequency registers in a DDS device, you can increase the phase-shifting resolution from 12 to 32 bits.

phase-shifting resolution becomes $360^\circ/2^N$, where N is the resolution of the frequency register. Many DDS devices have 32-bit-wide frequency registers. You can therefore phase-shift the output signal with a resolution of $(83.82 \times 10^{-9})^\circ$. For example, if register FREQ0 contains the output-frequency value, then you can set FREQ1 to $FREQ0 + Q$, thus phase-shifting the output signal by Q . Under normal conditions, FREQ0 supplies the phase accumulator of the DDS device. During phase-shifting, you select FREQ1 for one MCLK cycle, resulting in phase shifting the output signal by Q .

You can phase-shift the output signal by 0 to 360° . However, the frequency registers should not contain a value equal to or greater than 180° . Thus, to perform phase shifts greater than 180° , you must use the phase register along with the frequency register. You can set the phase register to 180° while using the frequency register to obtain the fine phase-shift resolution. The phase register and FREQ1 register serve as coarse and fine tuners, respectively. You use both registers in unison to perform the phase shift. For example, for Q phase shift in the out-

put signal, $PHASE + FREQ1 = Q + FREQ0$. You set $PHASE$ to 180° and $FREQ1$ to $Q + FREQ0 - 180^\circ$.

A DDS device has associated pipeline delays. When you select a frequency or phase register, a pipeline delay exists before you see a change at the DAC's output. In some devices, the latency from the phase register to the DAC's output is different from the latency from the frequency register to the DAC's output. With such devices, an intermediate phase shift occurs because the phase shift from either the FREQ1 or PHASE register occurs before the phase shift from the other register. In other DDS devices, such as the AD9830 and AD9831, the latency from the frequency and phase registers to the DAC's output is the same. Therefore, no intermediate phase shift occurs. The plot in **Figure 2** shows the performance of the circuit in **Figure 1**, using the AD9830/9831 DDS device.

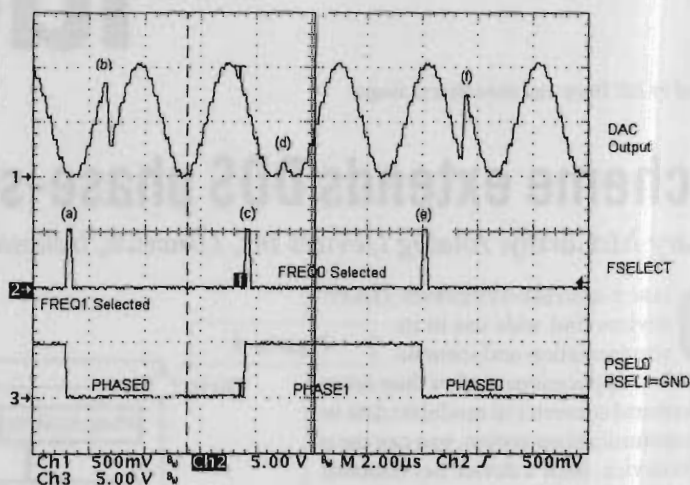
The master clock to the DDS device runs at 5 MHz. The device generates a 312.5-kHz output signal. The phase shift of the output signal is 270° at points b, d, and f in the plot. Because the PHASE register in the DDS device comes after

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the numerically controlled oscillator (NCO), you must keep this register selected until the next phase shift takes place. The FREQ1 register comes before the NCO, so you need to select it for only one MCLK signal. The AD9830/9831 has four phase registers, so you can use two of them to perform the phase-shifting. For the plot in **Figure 2**, PHASE0 and PHASE1 are the selected registers. At Point b, the output phase shift is 270° . PHASE0's setting is 2048— 180° , whereas FREQ1's setting is 1.5625 MHz (equivalent to $312.5 \text{ kHz} + 90^\circ$). Selection of FREQ1 and PHASE0 occurs at Point a, with FREQ1's selection lasting one MCLK cycle, and PHASE0's selection a continuous one.

At b, the phase and frequency values have propagated through the DDS device, causing an output phase shift of $180 + 90 = 270^\circ$. At c, FREQ1's selection lasts one MCLK cycle, and PHASE1 becomes selected, with a value of zero. PHASE1 causes an output phase shift of

Figure 2



Points b and c show the output waveform shifting in phase by 270° .

-180° (PHASE1—PHASE0 = $0 - 180^\circ$). At d, the output signal's phase shift is $-180 + 90 = -90 = +270^\circ$. At e, FREQ1 becomes selected for one MCLK cycle while PHASE0 is again selected. This se-

lection produces an output (f) phase shift of $180 + 90 = 270^\circ$. (DI #2387).

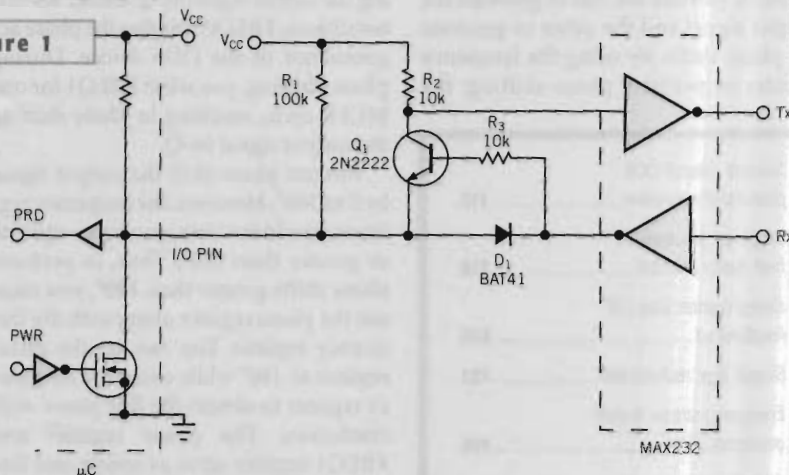
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Single μC pin makes half-duplex RS-232C

By Marin Ossman, University of Applied Sciences, Aachen, Germany

IN MANY μC DESIGNS, nearly all the I/O pins are occupied. If only one I/O pin is available, the circuit in **Figure 1** can help you implement a serial RS-232C interface. For many purposes, half-duplex operation using a software-driven RS-232C interface provides a good communications link. Many μCs have open-drain I/O pins, as shown on the left of the figure. In the idle state, the RS-232C lines Rx and Tx both assume a negative voltage; their TTL counterparts assume a high level. The I/O pin is also at a high level, and neither D_1 nor Q_1 conduct. If a mark signal on the Rx line pulls the Rx line high, D_1 conducts, the I/O pin goes low, and the μC reads this low level. Because the base of Q_1 is negative with respect to its emitter, Q_1 does not conduct and Tx does not retransmit the mark level. If the μC wants to transmit a mark, it pulls the I/O pin low (by setting power to low).

Figure 1



An unused I/O pin in a μC provides a convenient way to implement an RS-232C communications link.

Now the emitter of Q_1 is at ground level, and the high level on the Rx interface output supplies base current to Q_1 via R_3 . Q_1 conducts, and the RS-232C Tx driver input goes low. The MAX232 driver transmits a high-level mark signal. In this way, Q_1 and D_1 simply provide a route from Rx to the I/O pin when the circuit receives characters without echoing

them, and the μC itself also transmits characters. R_1 is necessary only if no internal pullup resistor is available. You can use this type of circuit for service purposes in many designs, such as to connect a PC to a pin of a μC . At startup, the μC sends a short message to the PC. Then, the PC sends initialization or debugging parameters to the μC . During normal

operation, the μC reports its actions to the PC by transmitting the appropriate data. If the circuit has a pin with edge-triggered interrupt capability, you can even implement interrupt-driven I/O. (DI #2397).

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Binary counter uses LSB feedforward

Robert Carter, Siemens PLC, Congleton, Cheshire, UK

A TYPICAL SYNCHRONOUS BINARY counter contains a series of flip-flops, each of which changes state when all least significant bits (LSBs) are logic 1. This repeated AND function is the Achilles' heel of the binary counter. A designer has two choices: Use a ripple AND function (Figure 1), or a parallel AND function (Figure 2). The ripple AND function is slow, but the parallel AND function is hugely wasteful of gates and places a large fan-out burden on the LSBs of the counter. Note that, in typical CMOS gate-array technology, AND gates

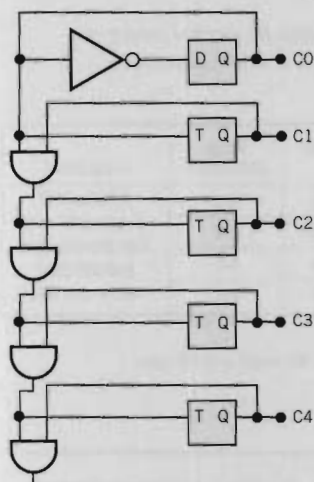
with more than four inputs are made up of combinations of gates. The configuration in Figure 3 combines the best features of both approaches.

The key to combining the two methods is to recognize that an AND function, *not* including the LSB of the counter, has two whole clock cycles to complete and then simply bring in the LSB in parallel with a further two-input AND gate. The approach in Figure 3 is generally beneficial when the counter is wider than 6 bits. This application is for a 32-bit error counter using 2- μm CMOS or a 140-

Mbps plesiochronous-digital-hierarchy test set. You can extend the technique (to more than 15 bits or so) to propagate the LSBs in parallel; this extension would give the ripple path four clock cycles to settle. The downside of this method is that next-state errors would occur if you needed a resettable counter, though you can usually design out the requirement for such a counter at the system level. (DI #2388)

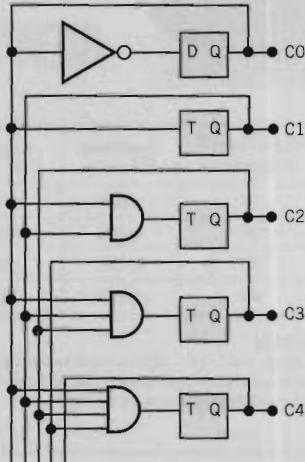
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Figure 1



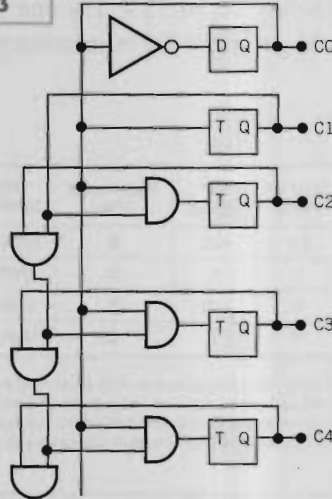
The ripple AND architecture is slow but economical of gates.

Figure 2



The parallel AND configuration is faster than the ripple AND technique but is wasteful of gates.

Figure 3



An LSB-feedforward technique combines the best features of the ripple- and parallel-AND methods.

Simple logic reduces EMI

Eugene Palatnik, BCI International, Waukesha, WI

A CURRENT-INPUT ADC whose primary use is measuring low-level signals from photodetectors can also measure a range of voltages using the circuit in **Figure 1**. The main component is a dual-input current-integrating ADC, IC₁. IC₂ and IC₃ provide the buffered 4.096V reference for IC₁. The figure does not include a μ C, which typically oversees the digital control and data retrieval.

When you use IC₁ with photodetectors, this ADC integrates the currents at input pins 1 and 28 for a user-controlled integration period, T_{INT} . IC₁ then digitizes the output voltages of the integrators into 20-

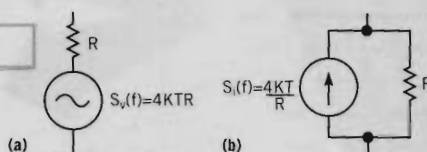
bit digital words that are ready for retrieval over the serial interface. The only modifications necessary to enable IC₁ to measure voltages are resistors in series with the inputs. IC₁'s integrators hold the

input at a virtual ground, so the applied voltages produce currents through the resistors, which by Ohm's law equal V_{IN}/R_{INPUT} . The full-scale voltage input for the circuit in **Figure 1** is

$$V_{INFS} = I_{FS} R_{INPUT} = \frac{Q_{FS}}{T_{INT}} R_{INPUT}$$

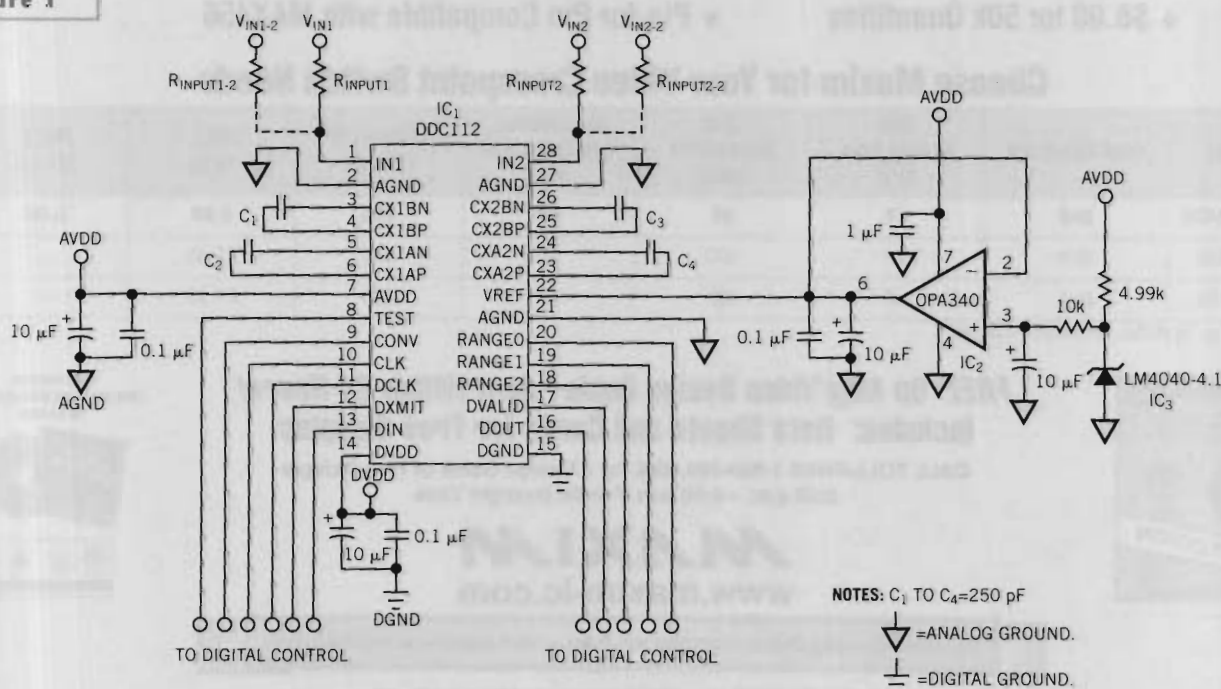
where I_{FS} is the full-scale input current; Q_{FS} is the full-scale range of IC₁ in coulombs, set by pins RANGE₀ to RANGE₂; and T_{INT} is the user-controlled integration period. R_{INPUT} 's value should be large, preferably greater than 10 M Ω . Avoid using resistors with poor voltage co-

Figure 2



The spectral density of the voltage noise, $S_v(f)$, is proportional to the value of resistance (a), but the spectral density of the current noise, $S_i(f)$, is inversely proportional to the value of resistance (b).

Figure 1



NOTES: C₁ TO C₄=250 pF
 =ANALOG GROUND.
 =DIGITAL GROUND.

Series input resistors allow a current-input ADC to measure a wide range of voltages.

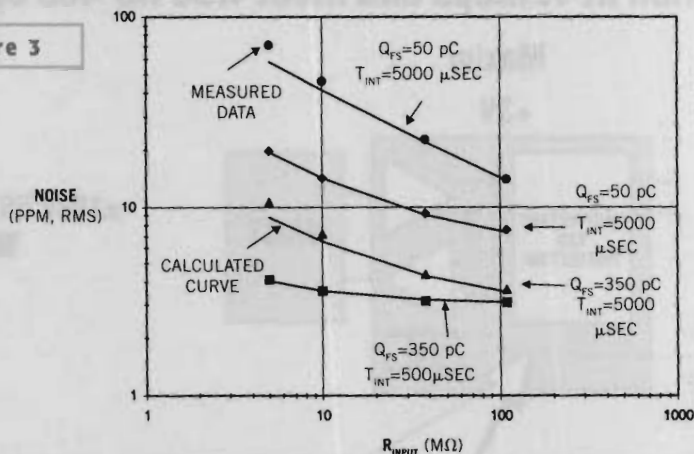
efficient and excess noise. Caddock Electronics Inc (www.caddock.com) offers a variety of high-value resistors with good performance.

Eight full-scale ranges are available in IC₁. Seven of these ranges are internal ranges of 50 to 350 pC in steps of 50 pC. The eighth range uses external capacitors C₁ to C₄ to establish a full-scale range of approximately $0.96 \times V_{REF} \times C_{EXT}$. For the 250-pF capacitors in Figure 1, this external range is approximately 866 pC. Surface-mount COG capacitors are a good choice for C₁ to C₄. The CONV Pin of IC₁ sets the integration time. In a typical configuration, the minimum integration period for continuous operation is 500 μ sec, and the maximum period is 1 sec.

The circuit exhibits a number of useful features. First, the dynamic range of the circuit is large: IC₁ outputs 20-bit words. Adjusting Q_{FS} and T_{INT} provides additional dynamic range. The circuit can measure voltages that span more than seven orders of magnitude using a fixed value of R_{INPUT}. Second, the virtual ground at IC₁'s inputs allows you to place additional resistors in parallel, such as R_{INPUT1-2} and R_{INPUT2-2'} to measure the sum of the applied voltages. And, because IC₁ is a dual-input ADC, the circuit can simultaneously make two independent voltage measurements. Finally, the large-value resistors in series with IC₁'s inputs allow the circuit to measure large voltages. For example, if R_{INPUT}=100 M Ω , then a voltage of 100V produces only a 1- μ A current, which IC₁ can easily measure. When using large voltages, make sure that the resistors are rated to handle the voltages and that the pc-board layout provides the proper spacing for insulating the high-voltage lines.

At first glance, you might think that the large resistors in series with IC₁'s inputs contribute a lot of thermal noise. Fortunately, the noise that these resistors produce is usually low and decreases as the resistor values increase. To see why this surprising behavior occurs, consider two identical noise models of a resistor (Figure 2). The model in Figure 2a is probably more familiar and shows the

Figure 3



This plot of noise performance versus R_{INPUT} for different values of T_{INT} and Q_{FS} includes both measured and calculated results.

resistor modeled as a voltage source in series with a noiseless resistor. The spectral density of the voltage noise, S_v(f), is proportional to the value of resistance. The Thevenin-equivalent model in Figure 2b comprises a current source in parallel with a noiseless resistor. In this case, the spectral density of the current noise, S_i(f), is inversely proportional to the value of resistance. The bigger the resistance, the smaller the current noise. IC₁ measures current. The current-noise contribution of the resistor is important, so bigger resistors reduce the noise. Also, the thermal noise power is independent of resistance. (For a detailed explanation of the physics behind thermal and other noise phenomenon, see Reference 1.)

You can use the following expression to calculate the rms thermal noise, where V_{FS} is the integrator's full-scale voltage, not the input signal's full-scale voltage, V_{inFS}, in the previous equation:

$$\text{NOISE(ppm)} = 10^6 \frac{\bar{v}}{V_{FS}} = 10^6 \frac{\sqrt{\frac{2KT}{R} T_{INT}}}{Q_{FS}}$$

You must add this thermal noise to IC₁'s inherent noise to calculate the total rms noise. Figure 3 shows noise performance versus R_{INPUT} for values of T_{INT} and Q_{FS}. The figure includes measurement points for comparison with the calculated noise performance.

IC₁'s inputs have very high input impedances and can be susceptible to noise pickup unless you use care in laying out the circuit. Try to keep R_{INPUT} as close to the inputs as possible to minimize the length of the input traces. Also, shield the input leads and IC₁ with grounds wherever possible. If noise pickup is still a problem, adjusting the integration period can notch out specific frequencies. For example, setting the integration period to 16.666 msec places a notch in the frequency response at 60 Hz. (DI #2392)

REFERENCE

1. Van der Ziel, Aldert, *Noise in Solid State Devices and Circuits*, John Wiley and Sons, 1986.

TO VOTE FOR THIS DESIGN,
CIRCLE NO. 342

Emergency strobe flasher generates 250V

Robert Sheehan, Linear Technology Corp, Milpitas, Corp

FIGURE 1 SHOWS A COMPLETE circuit for an emergency lamp that operates from a 12V automotive battery. The xenon flash tube requires a 250V-dc anode voltage and a 4-kV trigger pulse. To generate the 250V dc, IC₁, a switching regulator controller, and T₁, a standard Versa-PAC transformer, operate in the discontinuous-flyback mode. With this configuration, circuit efficiency is typically 75 to 80%. R₁ and IC₁'s internal-sense-threshold voltage limit the peak primary current to 1.6A. The R₂/R₃ divider and IC₁'s internal 1.25V reference at the VFB Pin determine the maximum-voltage setpoint. To generate the 4-kV trigger pulse, a standard cold-cathode-fluorescent-lamp (CCFL) backlight

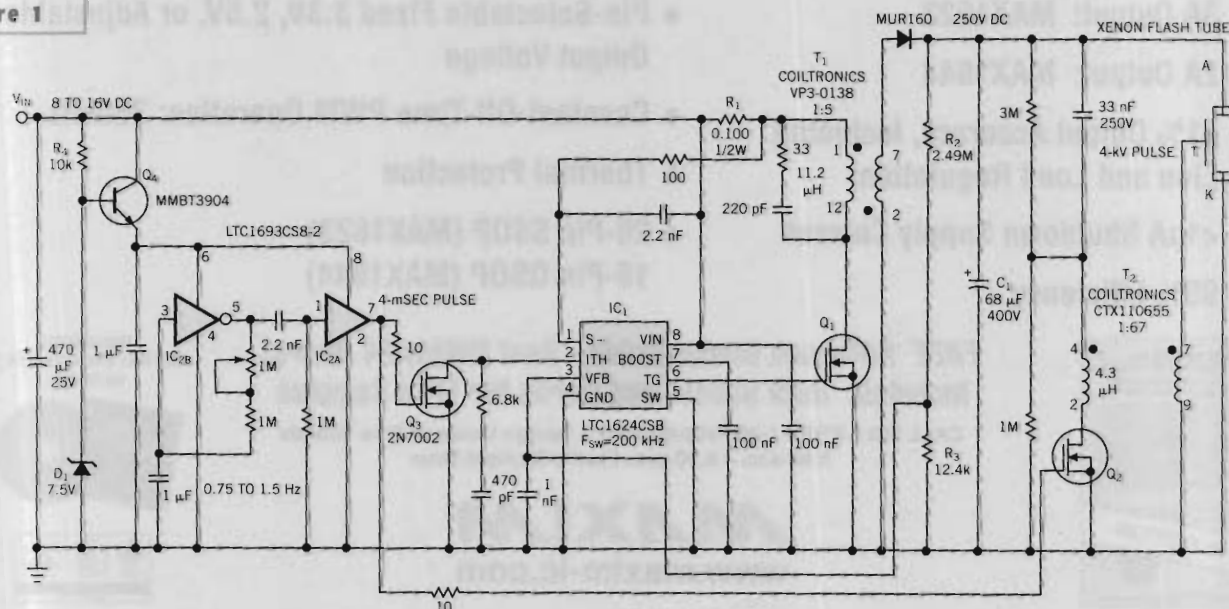
transformer, T₂, operates in the forward mode. IC₂, a dual MOSFET driver, functions as a 1-Hz oscillator and a one-shot for the trigger pulse for Q₂. Additionally, Q₃ blanks out the operation of the 250V supply during this time. This feature is important because the circuit must reduce the flash tube's anode current to a low level, allowing the tube to reset and wait for the next cycle. Otherwise, the Xenon flash tube may burn out.

The selected flash tube has a maximum flash energy of 4W/sec (joules) and a maximum frequency of 60 flashes/min. Using a 68-μF capacitor for C₁, the available flash energy, $\frac{1}{2}CV^2$, is 2 joules, and a flash frequency greater than 1 Hz is possible.

If input voltages below 8V are desirable—for example, when you use a 6V lantern battery—it is important to limit the flash frequency to less than 1 Hz. This limit allows sufficient time for C₁ to charge. The peak primary current, converter switching frequency, and transformer primary inductance determine the charge time: $t = (\frac{1}{2}CV^2)/(\frac{1}{2}LI^2f)$. You can omit Q₄, D₁, and R₄ and use V_{IN} to power IC₂. (DI #2393)

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Figure 1



NOTES: Q₁, Q₂—FAIRCHILD NDT410EL
FLASH TUBE—RADIO SHACK 272-1145
FOR T₁, CONNECT PINS 3 AND 11, 4 AND 10, 5 AND 9, AND 6 AND 8.

A complete circuit for an emergency lamp operates from a 12V automotive battery and generates a 250V-dc anode voltage and a 4-kV trigger pulse for the Xenon flash tube.

3.3V lithium-cell supply requires one inductor

Matt Schindler and Jay Scolio, Maxim Integrated Products, Sunnyvale, CA

BECAUSE OF THE GROWING popularity of lithium-ion (Li-ion) batteries and 3.3V power supplies, portable-equipment designers must often create a 3.3V supply that a single Li-ion cell can power. The fact that the output of a Li-ion battery ranges above and below 3.3V during its discharge cycle complicates the design.

This situation calls for a buck/boost converter, which can perform both step-up and step-down conversions. This requirement is not new; for years, portable-equipment designers have faced the similar problem of deriving 5V from the output of four NiCd cells.

Using a flyback converter is tempting, but the size and expense of a transformer and the extra noise that this converter type creates prompt the search for an alternative. For example, the single-ended primary-inductance converter (SEPIC) is quieter, but this converter's buck/boost circuit has a maximum limited efficiency

of 85%. This converter also requires either a transformer or two inductors in place of the single inductor that most dc/dc converters require.

You might overlook an alternative approach because the converter uses a linear regulator and takes an efficiency hit when you fully charge the Li-ion battery to about 4.2V (Figure 1). Nevertheless, this approach offers a longer battery life than the other two buck/boost circuits. For a large portion of the Li-ion battery's discharge cycle, battery voltage is within a range that allows the converter to exhibit excellent efficiency.

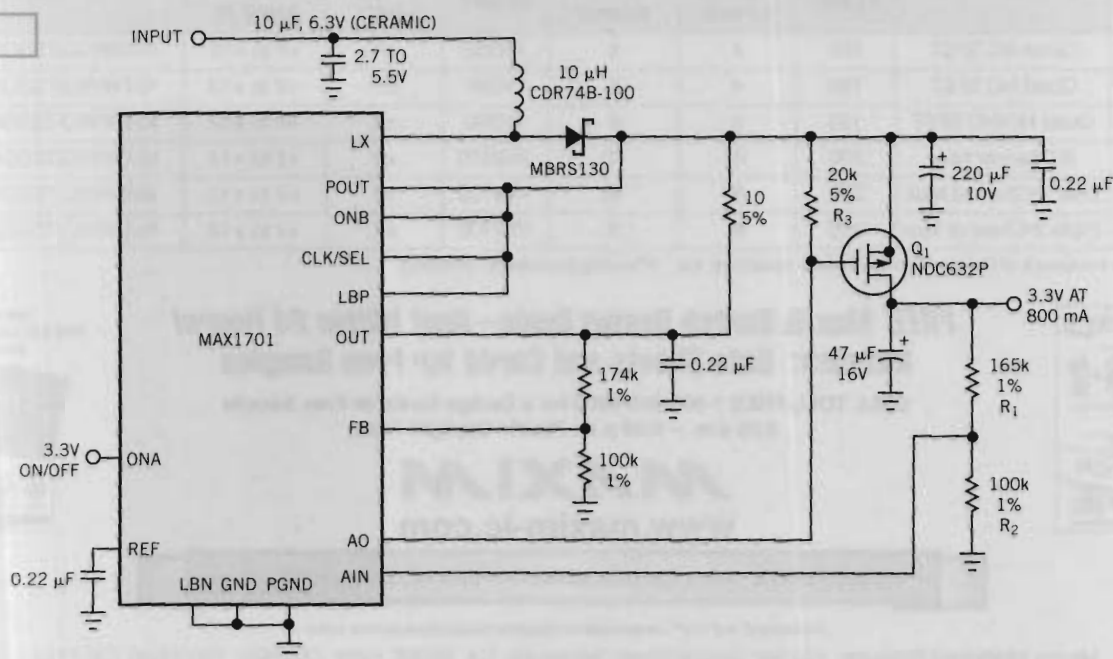
The operation of the circuit is straightforward. When the input voltage is above 3.3V, the IC stops switching. A linear regulator comprising Q_1 , R_1 , R_2 , R_3 , and an op amp internal to the IC step down the input voltage to 3.3V. When the input is below 3.3V, the IC operates as a step-up switching regulator and boosts the output to 3.3V. For this condition, the MOS-

FET is fully on, offering a virtual short from drain to source.

Efficiency is a function of the input voltage and the output current. As expected, the efficiency is a minimum of approximately 78.5% for a peak battery voltage of 4.2V. However, with a 3.6V input and an output current of less than 500 mA, the efficiency is above 89%. This behavior is significant because the output of a Li-ion cell is nearly 3.6V for most of its discharge cycle. For inputs of 3.3 to 3.6V and the same output-current conditions, the efficiency is even higher. Efficiency is also in the same range when the IC operates as a step-up switching converter, which it does for battery voltages below 3.3V. The efficiency gradually decreases as the output current exceeds 500 mA. (DI #2390)

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Figure 1



This buck/boost circuit assumes the buck, or linear-regulator, mode for inputs above 3.3V and the boost, or switching-regulator, mode for inputs below 3.3V.